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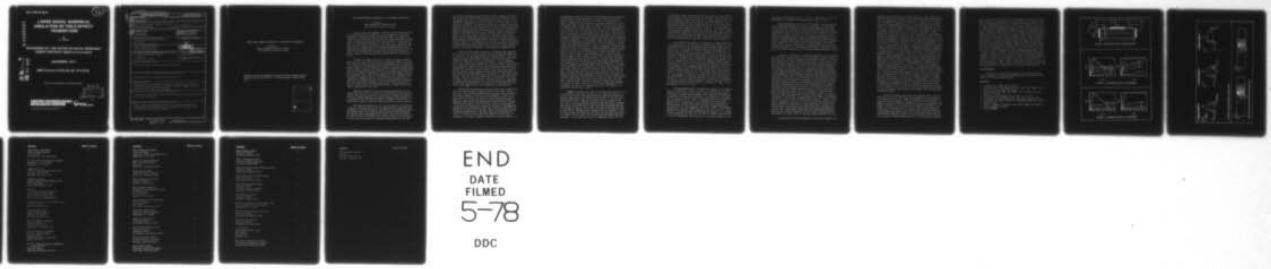

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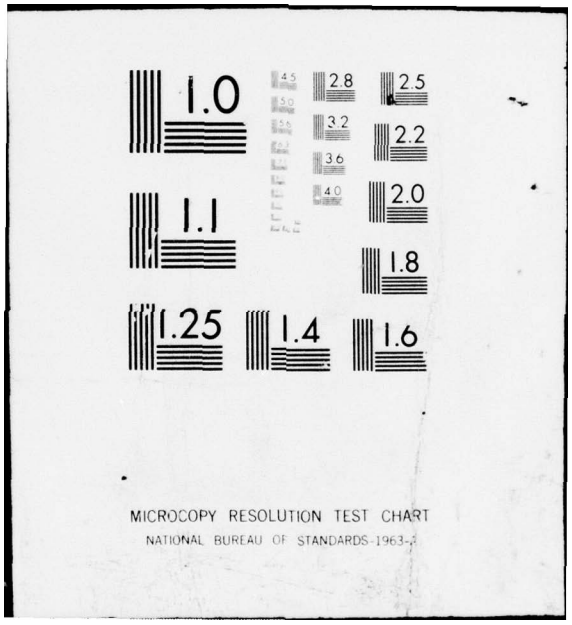
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LARGE SIGNAL NUMERICAL SIMULATION OF FIELD EFFECT TRANSISTORS

By
H.L. Grubin

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A large signal time dependent numerical code has been developed for simulating the space charge and circuit dependence of nonlinear single gate unipolar field effect transistors.

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Presented at the Sixth Biennial Conference on 'Active Microwave Semiconductor Devices and Circuits'. Cornell University, August 16-19, 1977.

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A large signal time dependent numerical code has been developed for simulating the space charge and circuit dependence of nonlinear single gate unipolar field effect transistors (FET). One goal of the simulation is to determine the ways the nonuniform space charge distribution is affected by the form of the velocity electric field relation, v(E), and the material properties of the device (e.g., substrate); and how it in turn affects such things as the source-drain current voltage characteristic. Another goal is to obtain design parameters for the large and small signal behavior of the FET. In the discussion that follows we will concentrate on the former goal and restrict ourselves to effects common to GaAs FETs possessing either Schottky[1] or junction[2] gates.

The FETs of interest fall into two groups according to whether under zero gate bias conditions they are or are not capable of sustaining a current instability arising from the propagation of a dipole layer. It is known that for sufficiently wide channel structures the devices exhibit, above a critical drain bias, microwave frequency oscillations[2,3]. The oscillation properties are dependent on the values of the drain and gate bias, and may be suppressed at sufficiently high negative gate[3] or positive drain[2] bias levels. Upon suppression of the oscillation normal FET operation appears possible. The oscillations do not appear to be significantly dependent upon the level of the active region doping, as the results of references 2 and 3 in which instabilities were observed were for significantly different doping values. The second group of FETs of interest are narrow channel devices and in these devices large signal instabilities do not occur.

Numerical simulation of the time dependent properties of wide channel GaAs FET in which the effects of the external circuit was included and the oscillation detected by variations in current and voltage across an external impedance was recently reported[4]. These results will be summarized below and used as a point of comparison with the more recent narrow channel studies and with studies that include a substrate.

The numerical simulation is for the device/circuit configuration of figure 1. The simulation is for two space dimensions plus time. The x-dependence is along the length of the channel, the y-dependence along the channel height. All variations along the z-direction are ignored. The calculations are performed for two cases: one in which the source and drain contacts are parallel (bold lines in figure 1) and the second in which all three contacts are coplanar (dashed lines). In all cases

the contacts are equipotentials. The active region height of the FET is denoted by H_c and that of the substrate by H_s. For the present study the doping within the active region and substrate are uniform and time independent. The doping of the active region is $10^{15}cm^{-3}$, that of the substrate is $10^{12}cm^{-3}$. The numerical results are not qualitatively dependent on the value of the doping within the active region, and the low value was chosen to reduce computing costs. The specific semiconductor properties are represented by a field dependent velocity and diffusion relation. We assume an'instantaneous' velocity response to changes in electric field. This neglect of velocity 'overshoot' contributions means that the fundamental frequency limitation of the FET cannot be ascertained within the present program. Rather the frequency response obtained herein must be regarded as a lower limit to the true frequency response. Details of the parameters used in the calculation, references for the v(E) and diffusion curves, and a discussion of the numerical methods is contained in reference 4. The results are summarized next.

The static and dynamic properties of a Schottky gate GaAs FET with H_c=2.20 microns, L_g=1.95 microns and L=10 microns are summarized in figure 2a[4]. For this case the gate is centrally placed, the source and drain contacts are parallel and H_s=0. The results are essentially symmetrical about the bottom of the device; and it is as though a fictitious 'reflecting' substrate were present. Figure 2a displays drain current versus drain voltage for the device. Closed circles denote time independent computed points; crosses denote average current and voltage when the device is sustaining a self-excited transit time oscillation. The v(E) curve is also included in the diagram and scaled to the current and voltage parameters. The current is in multiples of $I_p = N_0 e v_p A$, where N_0 is the active region doping level, v_p the peak carrier velocity, and A the cross sectional area in the y-z plane. The drain potential, which is the potential on the drain contact is in multiples of $V_p = E_p L$, where E_p is the electric field at peak velocity. Here E_p= 3.2kV/cm and $v_p = 2.2 \times 10^7$cm/sec. The curves are further labelled by the value of gate bias, which is also expressed as a multiple of V_p.

The results associated with figure 2a teach that for each curve, and below saturation,that a depletion region exists under the gate contact and that the regions between the source and gate, and gate and drain may be regarded as electric-field-independent resistors. For V_{GO}=0 saturation begins at a value of drain potential significantly below that value of gate bias needed to reduce the drain current to negligibly small values. For the parameters associated with figure 2a the gate bias needed to pinchoff the drain current is approximately $-3.0V_p$(see also reference 3). Saturation for V_{GO}=0 is accompanied by the presence of an accumulation layer that forms within the conducting channel at the drain side of the gate contact. The accumulation layer is preceeded downstream by a depletion layer and dipole formation results. It should be noted that dipole formation for FETs is not a consequence of a region of negative differential mobility (NDM); it is

a consequence of velocity limitation[5] and channel widening downstream from the gate contact. The effects of dipole formation should also manifest itself in FETs fabricated from silicon. The presence of a region of NDM affects the stability of the dipole layer and for sufficiently high values of drain bias an instability occurs in the form of a propagating and recycling high field domain. The oscillation frequency is determined by the nucleation time under the gate, propagation time and drain time. For an average drain potential of $1.3V_p$ the frequency of oscillation is approximately 18GHz. The transit time oscillation is bias dependent and at sufficiently high values of drain bias the oscillation ceases and the space charge distribution within the FET now includes the presence of an accumulation layer that extends, within the conducting channel,from the drain side of the gate contact to the drain contact. One important consequence of this is that the region between the gate and drain contacts can no longer be modelled by a field independent resistance. The presence of charge accumulation between the gate and drain contacts is a consequence of a potential drop sufficiently great for the electrons to be travelling at their saturated drift velocity value v_s which is approximately equal to $0.4v_p$. Then,any significant value of drain current in excess of $0.4I_p$ would be expected to be accompanied by carrier accumulation. (Similar high bias space charge distributions are thought to be responsible for the amplification properties of two terminal super-critical amplifiers[6].) The situation at moderately increased negative values of gate bias is similar to that for $V_{GO}=0$, but at sufficiently high values the oscillations again cease. For this case the low value of drain current implies that most of the potential drop must fall under the gate contact, and the regions between the source and gate and gate and drain can again be regarded a electric field independent resistors. But an increased drain potential under large negative values of gate bias causes the depletion layer to migrate toward the drain contact with the result that the gate to drain parasitic resistance although no longer field dependent is dependent on bias. We point out that the gate dependence of the oscillation for the FET is a feature essential to the operation of transferred electron logic devices[7].

Parallel calculations to those for GaAs were performed on a fictitious element whose high field velocity is constant and equal to v_p for values of electric field greater than E_p. This zero differential mobility (ZDM) element has characteristics similar to that of silicon, although among other things its saturated velocity is greater than twice that of silicon. The ZDM calculations were performed to determine the extent to which NDM affects saturation; and also because the ZDM calculations are easily scaled, they can provide modelling assistance. For the ZDM calculations the diffusion was taken as constant and equal to 200 cm^2/sec. The ZDM current voltage curves are displayed in fig. 2b, where we have also drawn the v(E) curve. We note again that saturation begins, for the $V_{GO}=0$ case, at drain potential values below that necessary to pinch the drain current to negligible values. For this

case pinchoff occurs for a value of gate bias equal to $-2.5V_p$. Qualitatively similar results were obtained in reference 5. We also point out that the value of drain current, for $V_{GO}=0$, at high values of drain potential (exceeding those of the scale of figure 2b) approaches unity. This suggests that the device dimensions are not limiting the current values in the figure 2a GaAs calculations; rather it is the value of the high electric field saturated drift velocity. Additional calculations have been performed in which the saturated drift velocity values in NDM elements bracketed the GaAs value. For the case where the saturated drift velocity exceeded the GaAs value the high drain potential current level exceeded that for GaAs; the reverse occured for NDM elements with saturated drift velocities values less than the GaAs one.

One necessary requirement for the presence of large signal domain instabilities is that the current density be high enough to sustain a propagating domain. By decreasing the channel height the relative contribution of the depletion region under the gate increases and the current density throughout the device decreases. The elimination of domain instabilities is then possible . The question is: how much of a decrease is necessary. For the gate length of figure 2a the peak current, prior to saturation and the subsequent current instability, is very close to the minimum current necessary for supporting a traveling domain. This suggest that a device with with a somewhat smaller channel height would be sufficient for eliminating the instability. We did not do a systematic study of channel height versus stability. Instead for a channel height of 1.22 microns numerical simulations did not yield any large signal instability. The drain current versus drain voltage relation for this narrower device, with parallel source and drain contacts is displayed in figure 3a. In figure 3b we show computed results for a ZDM element with the same dimensions. We note for the figure 3 calculations that the voltage at the onset of saturation is approximately equal to the gate voltage necessary to pinchoff the drain current. For the GaAs element pinchoff occurs at a gate bias of $-0.6V_p$; for the ZDM element it occurs at $-0.6V_p$.

A cursory examination of the results of figures 2 and 3 suggests that if the presence of current instabilities is ignored in the three terminal device then the drain current versus drain voltage relation and perhaps the small signal parameters for a GaAs FET can be modelled by assuming a two piece velocity electric field relation of the type used in figures 2b and 3b. Indeed if the peak velocity for the ZDM element was chosen from a best fit with experiment then satisfactory agreement with the GaAs drain current versus drain voltage relation can be obtained. We have found that the current voltage relation in saturation and for time independent conditions submits to the relation $I_D=I_{DO}(V_D)(1 - V_{GO}/V_{GP})^n$, where $I_{DO}(V_D)$ is the drain current for $V_{GO}=0$, and V_{GP} is the value of gate bias necessary for pinchoff. n is a dimensionless parameter. The values of the pinchoff voltages have been given in the above paragraphs. The values of n for the GaAs elements in fig-

ures 2a and 3a are respectively 2.3 and 1.7 . The values of n for the ZDM elements in figures 2b and 3b are respectively 1.5 and 1.8 .

There are,however, limitations in the extent to which a GaAs FET can be adequately modelled by a two piece ZDM element. In particular difficulties arise in representing the voltage dependence of the gate to drain resistance for the situation when there is significant charge accumulating within this region. In this case the distribution of charge within a wide channel GaAs FET (see figure 8 of reference 4) is not necessarily the same as that within a wide channel ZDM element. The situation is somewhat brighter for narrow channel devices where the drain current is significantly below the current associated with the saturated drift velocity. In this case for both the GaAs element and the ZDM element saturation is accompanied by a large potential drop under the gate region, where most of the charge nonuniformities reside. We illustrate this charge distribution for the narrow channel GaAs FET in figure 4.

In figure 4 we display, for three combinations of drain potential and gate bias, the projection of the carrier density within the FET. We note that carrier density increases in the downward direction. In figure 4a the gate bias is zero and the drain potential is $0.28V_p$. We point out that the rate of increase of mobile carrier density under the gate contact is greatest near the source side of the gate region. In figure 4b the results for a drain potential of $0.72V_p$ show the rate of increase to be greatest at the drain side of the gate region where an accumulation of charge has formed. We note the region of partial carrier depletion downstream from the accumulation layer and the presence of the resulting dipole layer. Figure 4c shows the carrier density projection for a gate bias of $-0.3V_p$ and a drain potential of $1.93V_p$. Here the increase in negative gate bias results in a decrease in current density between the source and gate contacts, and between the gate and drain contacts. The region surrounding the gate is essentially swept free of mobile carriers.For the calculation of figure 4c, the low drain current and high drain potential values require that most of the potential drop be across the depletion region. This is illustrated in figure 5a which shows the large potential drop across the depleted region; the latter extending itself downstream from the gate contact region. The display in figure 5a is a contour plot of equipotential lines. Each line separates the regions $0.105r < V/V_p < 0.105(r+1)$, where r=0,1,2,...,9,A,B,... Lines A,B,C,.. represent r=10,11,12,.. We point out that the potential drop across the depletion zone results in an average electric field sufficiently high for the carriers to be traveling at their saturated drift velocity value. We indicated above that the potential and charge distribution for a narrow channel ZDM element was qualitatively similar to that for GaAs. Figure 5b displays a contour plot of potential for the ZDM element with a gate bias of $-0.2V_p$ and a drain potential of $1.34V_p$.

The calculations we have performed are time domain transient cal-

culations and so far have not revealed a region of static negative differential conductivity. Instead a low voltage high current state may switch to a lower current higher voltage state through an unstable region. The time dependent calculations in addition to allowing us to explore the transit-time dependent properties of the three terminal device, also allow us to explore the large signal amplification properties of the device, and to obtain realistic estimates of the response of the system to changes in gate and drain bias. In figure 6 we display a large signal gate current versus time profile, where time is in multiples of the low field dielectric relaxation time, 0.9×10^{-12} sec for 10^{15} doping. We show in a sequence of steps the time it takes the carriers to settle into a time-independent distribution after responding to changes in bias. At time t=0 the device is turned on with the gate bias decreasing at a finite rate to the value $-0.2V_p$ and the drain bias increasing at a finite rate to the value $0.5V_p$. There is initially a transient displacement current contribution due to these bias changes which results primarily in charge buildup on the gate contact. Conduction current contributions are always present but they dominate after the bias has reached its assigned value. In this case the conduction current contributions correspond to charge rearrangement within the device as determined by the amount of charge residing on the gate contact. Charge rearrangement is represented in figure 6 by the apparent exponential relaxation of the gate current to a zero value. The relaxation to steady state is dependent upon the speed of the carriers, the width of the depletion region and parasitic contributions. Going to higher drain bias values results in an increase in carrier velocity for situations below saturation. The result is a decrease in the time of relaxation. This is displayed in figure 6 where at the normalized times of 80 and 120 the drain bias is increased at a finite rate to the values $1.0V_p$ and $1.5V_p$, respectively. An increase in the value of the gate potential to a higher negative value results in an increase in the resistance of the device. The result is an increase in the time the system takes to settle into a steady state configuration. This is illustrated in figure 6, where at the normalized time of 160 the gate bias is decreased from the value $-0.2V_p$ to the value $-0.4V_p$. In this case the drain bias was held fixed at $1.5V_p$. We note that the calculations of figure 6 were for the narrow channel ZDM element.

The above discussion has ignored all substrate effects, except isofar as the bottom of the device may be regarded as the boundary line to a 'reflecting' substrate . Below, we briefly discuss some aspects associated with the presence of a substrate, and for this situation the numerical calculations are for the FET in the planar configuration. With respect to figure 1, L =10 microns and the height of the FET is 1.76 microns. H_c=0.98 microns, H_s=0.59 microns with the doping transition occuring over the distance of 0.19 microns. The source, gate and drain contact lengths are respectively 0.59, 1.59 and 1.76 microns. The calculations are displayed in figure 7 and are intended to draw attention to the presence of space charge injection into the substrate. The place-

ment of the contacts is indicated on the diagram. In figure 7 we display carrier density contours where the contours separate the regions $0.263 < N/N_0 < 0.263(r+1)$ for $N_0 = 10^{15}/cm^3$. We also show potential contours, which for figure 7a separate the regions $0.263r < V/V_p < 0.263(r+1)$; for figure 7b they separate the regions $1.05 < V/V_p < 1.05(r+1)$. We also display a set of current density streamlines through the device. The streamlines represent the vector current density, with the length of individual streamlines proportional to the magnitude of the current density. The maximum length of the individual x- and y- components before overlap is equal to J_p in figure 7a and $\frac{1}{2}J_p$ in figure 7b, where $J_p = N_0 e v_p$. The computation in figure 7a is for a zero gate bias and a drain potential of $2.68V_p$. Here we see the presence of charge accumulation under the gate region near the n-region/substrate boundary. There is also some current transport from the n-region into the substrate at the source end of the FET. But under the gate region all current is parallel to the bottom of the device; i e., the y- component of current is approximately zero. There is however enough structure in the potential at the n-region/substrate boundary to yield a finite y-component of electric field and consequent injection of carriers into the substrate. Once in the substrate they may contribute to the conduction current. Conduction in the substrate is also illustrated in figure 7b where the gate bias is equal to $-0.2V_p$ and the drain potential $1.87V_p$. For this case there is almost no current flow through the n-region; instead most of it is within the substrate.

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REFERENCES

1. C.A.Mead, Proc. IEEE., 54, 307 (1966).
2. H.R.Winteler and A.Steinmann, Proc. Int. Symp. GaAs (1966), Inst. of Phys. Conf. Ser., London, 228 (1967).
3. R Zuleg, Proc. Int. Symp. GaAs (1968), Inst. of Phys. Conf. Ser., London, 181 (1969).
4. H.L.Grubin and T.M.McHugh, Sol. St. Elect. (in press).
5. D.P.Kennedy and R.R.O'Brien, IBM J. Res. Devel., 14, 95 (1970).
6. R.Spitalnik, M.P.Shaw, A.Rabier and J.Magarshak, Appl. Phys. Letts., 22, 162 (1973).
7. G.Goto, T.Nakamura, K.Kayetani, and T.Isobe, IEEE Trans. Electron Devices, ED-23, 21 (1976).
8. To be published.

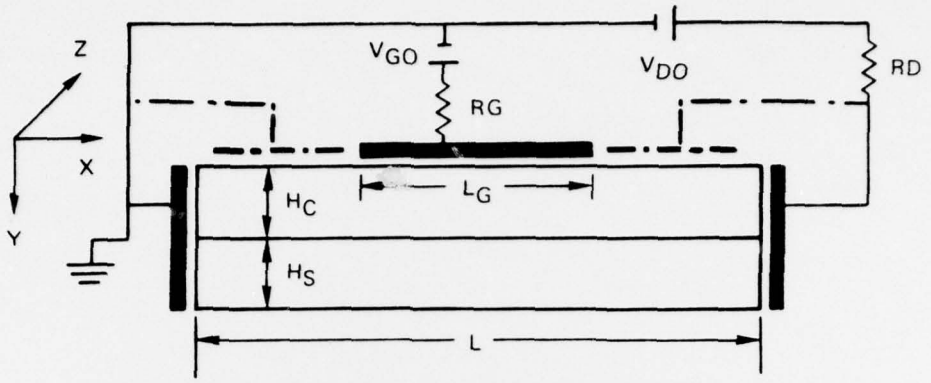


FIGURE 1. DEVICE AND CIRCUIT CONFIGURATION

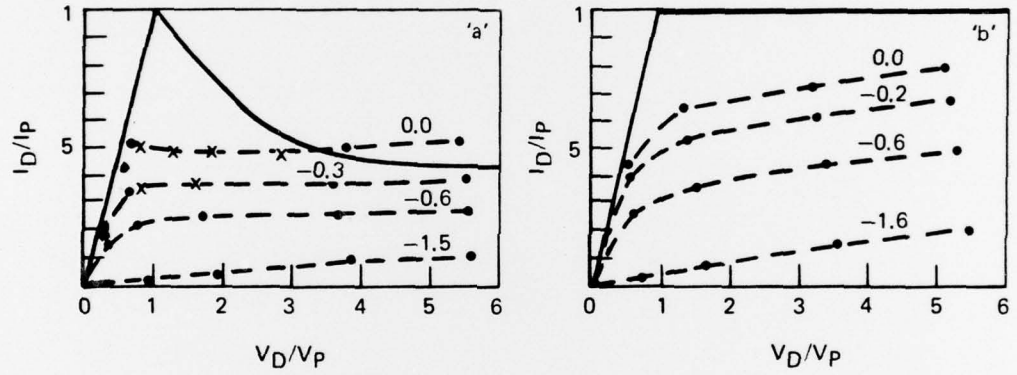


FIGURE 2. I_D VERSUS V_D FOR H_C = 2.24 MICRONS

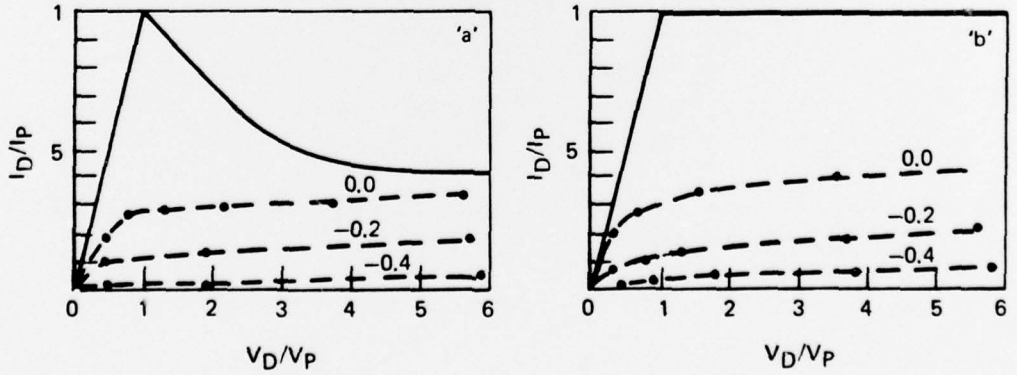


FIGURE 3. I_D VERSUS V_D FOR H_C = 1.22 MICRONS

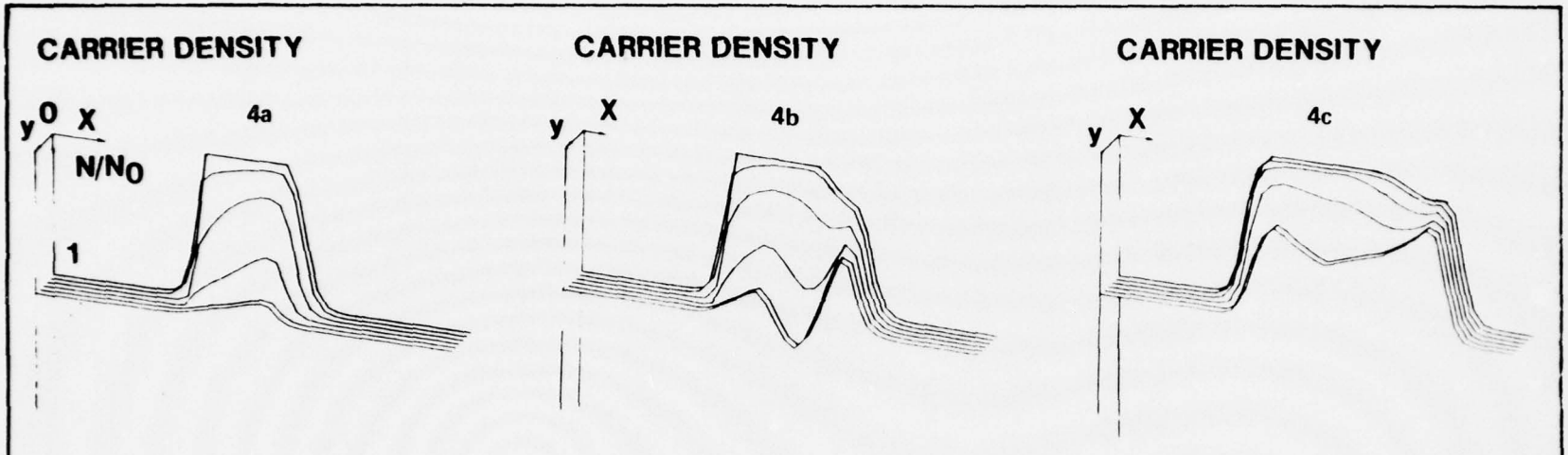


FIGURE 4. CARRIER DENSITY PROJECTION

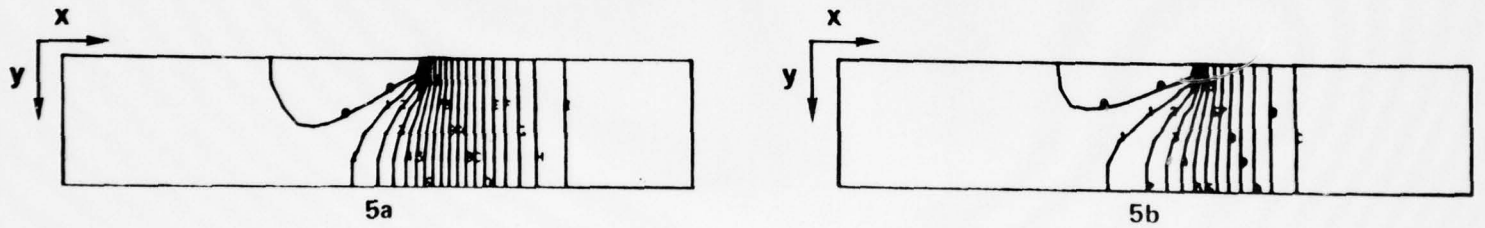


FIGURE 5. POTENTIAL CONTOUR DISTRIBUTION

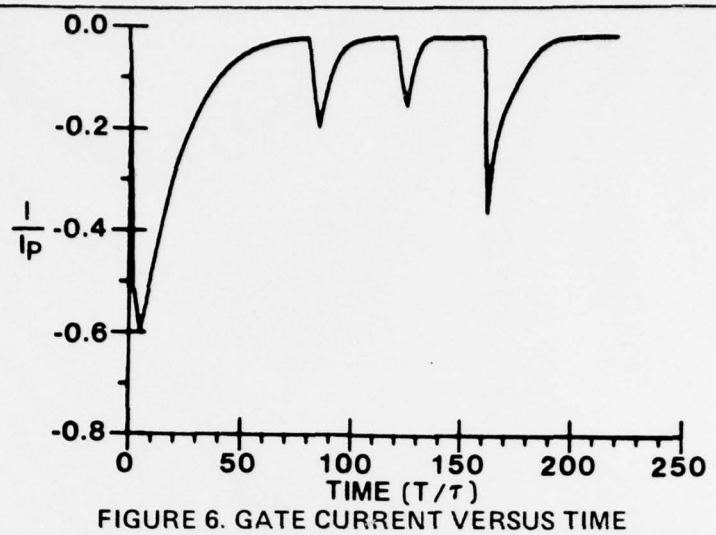
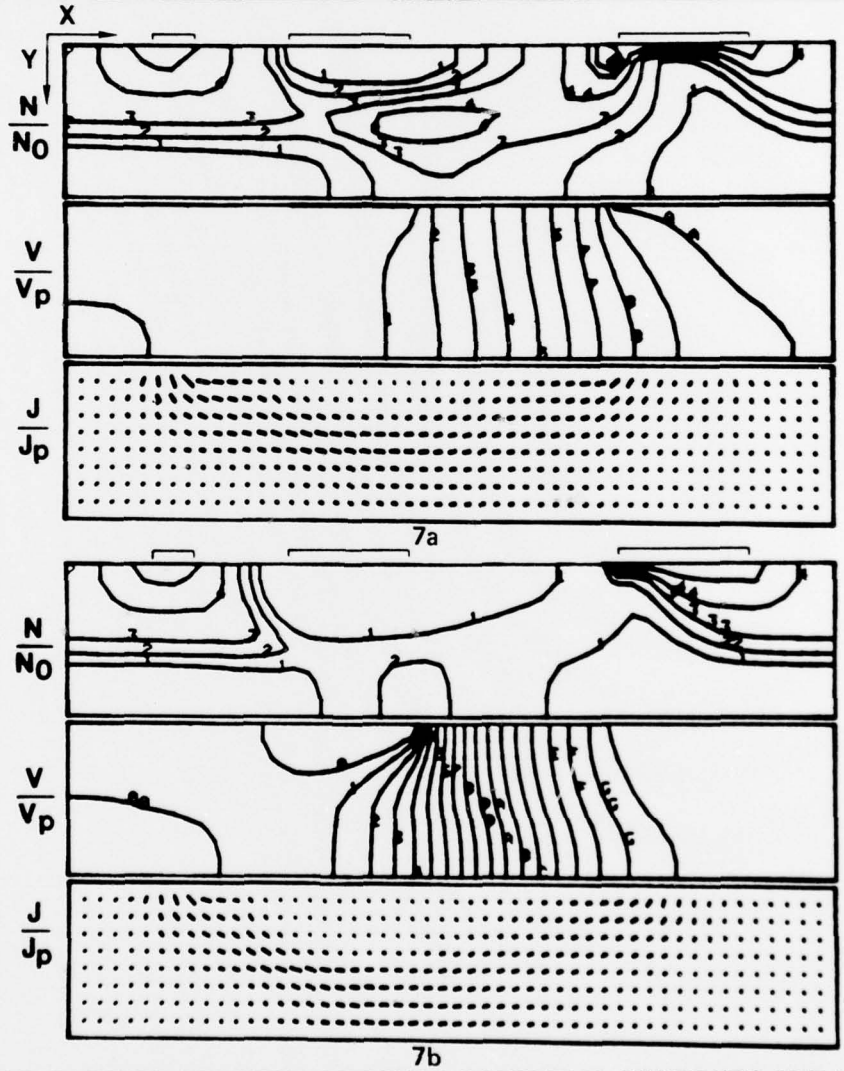


FIGURE 6. GATE CURRENT VERSUS TIME



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